IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the Abstract comprising lines 1-22 of page 18 with the following:

~~**A LOW-COST HIGH-SPEED MULTIPLIER/ACCUMULATOR UNIT FOR DECISION FEEDBACK EQUALIZERS**~~

ABSTRACT OF THE DISCLOSURE

A multiplier device for multiplying one of a discrete set of digital level values with a filter coefficient in a filter device implemented in a decision feedback equalizer ~~comprises:~~including (i) a decoder device for receiving a discrete digital level value to be multiplied and for generating control signals according to the digital level value~~;~~, (ii) an inverter circuit providing two parallel operations, each operation including multiplying the determined number by either +1/-1 in accordance with the control signals for generating two intermediate results~~;~~, (iii) a multiplier circuit receiving the two intermediate results and providing respective parallel operations for multiplying a corresponding intermediate result by +1 or zero (0) in accordance with a control signal and generating further intermediate results~~;~~, (iv) a logic circuit for shifting bits of one further intermediate result to effect a multiplication of one of the further intermediate output result with a discrete digital level value different than any of the original plurality of discrete digital level values~~;~~, and, (v) an accumulator device for adding the results of the logic circuit shift multiplication with the further intermediate output result to obtain a final multiplication result. The multiplier device is implemented for performing convolution operations ~~is~~ with the filter and generating filter outputs implemented for reducing inter-symbol-interference in a communication system. The multiplier device advantageously achieves the desired multiplications for convolution operations using less semiconductor real estate, and at a greater speed and less redundancy.

Please replace the paragraph comprising lines 19-21 of page 7and lines 1 to 8 of page 8 with the following:

Figure 3 illustrates the low-cost, high-speed multiplier circuit 50 according to the invention. The multiplier circuit 50 includes: an inverter circuit 52 represented as XOR gates 54, 56 each for receiving bits of the number "y " to be multiplied and effecting a bit inversion depending upon the value of respective input control signals c1, c2; a sub-multiplication circuit 60 comprising AND gates 64, 66 each for receiving a respective output bits of XOR gates 54, 56 which comprise either an inverted or non-inverted version of the number "g ", and effecting a multiplication by either a 0 or a 1 depending upon the value of the respective input control signals c3, c4; and, a sub-multiplier circuit 70 which may be implemented as a two-input ~~multiplexor~~ multiplexer or shift circuit for receiving the output 68 of AND gate 64 and effecting a 4x or 8x multiplication to the result 68 by shifting bits depending upon the value of control signal c5.

Please replace the paragraph comprising lines 13-21 of page 10 and lines 1 to 4 of page 11 with the following:

After the right side and left side sub-multiplications have been carried out, the resulting outputs 74, 76 are simply added by accumulator mechanism ~~60~~ 80 which is a combined two-step carry-save adder structure for reducing the propagation time in the data path. Particularly, the two step adder structure 80 adds the sub-multiplication results 74, 76 and, the prior coefficient value 75 from the prior filter output which is stored in register 95. Accordingly, the carry save adder 80 provides a sum output 82 and carry output 85. These sum 82 and carry 85 output results are then input to a carry select/ripple adder circuit 90 which adds these results to provide a final filter output value for storage in register 95. As shown in Figure 3, the control signals c1 and c2 are input to the carry select/ripple adder circuit 90 and added to the least significant position of the sum 82 and carry 85 outputs to correct the bits for any inversion operation that is performed in the multiplier. Addition of the sum 82 and carry 85 output results is then input back to register 95 and stored as the new filter output.